CLAIMS

~~1. A method of manufacturing a semiconductor component comprising:~~

~~providing a substrate with a surface;~~

~~providing a layer comprised of undoped gallium arsenide over the surface of the substrate;~~

~~forming a gate contact over a first portion of the layer; and~~

~~removing a second portion of the layer to expose a portion of the surface of the substrate.~~

2. The method of claim 1 wherein:

providing the layer further comprises providing the layer with a thickness of approximately three to twelve nanometers.

3. The method of claim 1 wherein:

providing the layer further comprises providing the layer with a thickness of approximately six to nine nanometers.

4. The method of claim 1 wherein:

forming the gate contact further comprises exposing the second portion of the layer.

5. The method of claim 1 wherein:

removing the second portion of the layer exposes a portion of the substrate.

6. The method of claim 1 further comprising:

implanting source and drain regions into the substrate after removing the second portion of the layer.

7. The method of claim 1 further comprising:

implanting source and drain regions into the substrate before removing the second portion of the layer.

8. The method of claim 1 further comprising:

forming a spacer adjacent to the gate contact after removing the second portion of the layer.

9. The method of claim 1 further comprising:

forming a spacer adjacent to the gate contact before removing the second portion of the layer.

10. The method of claim 9 further comprising:

keeping a third portion of the layer underneath the spacer after removing the second portion of the layer.

11. The method of claim 1 wherein:

providing the substrate further comprises providing a delta-doped, heteroepitaxial semiconductor structure for the substrate.

12. The method of claim 1 wherein:

providing the substrate further comprises:

providing a support layer;

providing a buffer layer overlying the support layer;

providing a doping layer overlying the buffer layer;

providing a spacer layer overlying the doping layer;

providing a channel layer overlying the spacer layer; and

providing a barrier layer overlying the channel layer.

13. The method of claim 1 wherein:

forming the gate contact further comprises:

forming the gate contact on the layer.

14. The method of claim 1 further comprising:

implanting source and drain regions into the substrate;

annealing the source and drain regions after removing the second portion of the layer; and

forming source and drain contacts over the source and drain regions after removing the second portion of the layer.

15. The method of claim 1 wherein:

removing the second portion of the layer further comprises keeping the first portion of the layer underneath the gate contact; and

removing the second portion of the layer further comprises keeping the first portion of the layer undoped.

16. A method of manufacturing a semiconductor component comprising:

providing a delta-doped, heteroepitaxial semiconductor substrate with a surface, the delta-doped, heteroepitaxial semiconductor substrate comprising:

a support layer comprised of semi-insulating gallium arsenide;

a buffer layer comprised of undoped gallium arsenide overlying the support layer;

a doping layer delta-doped with silicon and overlying the buffer layer;

a spacer layer comprised of undoped gallium arsenide and overlying the doping layer;

an channel layer comprised of indium gallium arsenide and overlying the spacer layer; and

a barrier layer comprised of aluminum gallium arsenide and overlying the channel layer, the barrier layer forming the surface for the delta-doped, heteroepitaxial semiconductor substrate;

providing an undoped gallium arsenide capping layer having a thickness of approximately three to twelve nanometers and overlying the surface of the delta-doped, heteroepitaxial semiconductor substrate;

forming a gate contact over the undoped gallium arsenide capping layer, the gate contact covering a first portion of the undoped gallium arsenide capping layer and absent over a second portion of the undoped gallium arsenide capping layer;

removing the second portion of the undoped gallium arsenide capping layer after forming the gate contact to expose a portion of the surface of the delta-doped, heteroepitaxial semiconductor substrate;

forming a spacer adjacent to the gate contact;

forming source and drain regions in the delta-doped, heteroepitaxial semiconductor substrate; and

forming source and drain contacts over the source and drain regions after removing the second portion of the undoped gallium arsenide capping layer.

17. The method of claim 16 wherein:

forming the source and drain regions further comprises implanting the source and drain regions into the delta-doped, heteroepitaxial semiconductor substrate after removing the second portion of the undoped gallium arsenide capping layer; and

forming the spacer further comprises forming a multi-layered spacer adjacent to the gate contact after removing the second portion of the undoped gallium arsenide capping layer.

18. The method of claim 16 further comprising:

forming the source and drain regions further comprises implanting source and drain regions into the delta-doped, heteroepitaxial semiconductor substrate before removing the second portion of the undoped gallium arsenide capping layer;

forming the spacer further comprises forming a multi-layered spacer adjacent to the gate contact before removing the second portion of the undoped gallium arsenide capping layer; and

keeping a third portion of the undoped gallium arsenide capping layer underneath the multi-layered spacer after removing the second portion of the undoped gallium arsenide capping layer.

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19. The method of claim 16 wherein:

providing the undoped gallium arsenide capping layer further comprises providing the undoped gallium arsenide capping layer with a thickness of approximately six to nine nanometers.

20. The method of claim 16 wherein:

providing the delta-doped, heteroepitaxial semiconductor substrate further comprises:

providing the buffer layer on the support layer and consisting essentially of gallium arsenide;

providing the doping layer on the buffer layer and consisting essentially of silicon and gallium arsenide;

providing the spacer layer on the doping layer and consisting essentially of gallium arsenide;

providing the channel layer on the spacer layer and consisting essentially of indium gallium arsenide; and

providing the barrier layer on the channel layer and consisting essentially of aluminum gallium arsenide;

providing the undoped gallium arsenide capping layer further comprises:

providing the undoped gallium arsenide capping layer on the barrier layer;

forming the gate contact further comprises:

forming the gate contact on the first portion of the undoped gallium arsenide capping layer; and

removing the second portion of the undoped gallium arsenide capping layer further comprises:

removing the second portion of the undoped gallium arsenide capping layer to expose a portion of the barrier layer.

21. The method of claim 20 further comprising:

annealing the source and drain regions after removing the second portion of the undoped gallium arsenide capping layer,

wherein:

providing the undoped gallium arsenide capping layer further comprises providing the undoped gallium arsenide capping layer with a thickness of approximately six to nine nanometers.

22. A semiconductor component comprising:

a substrate with a surface;

a layer comprised of undoped gallium arsenide over a first portion of the surface of the substrate; and

a gate contact over the layer,

wherein:

the layer is absent over a second portion of the substrate.

23. The semiconductor component of claim 22 wherein:

the layer has a thickness of approximately six to nine nanometers.

24. The semiconductor component of claim 22 wherein:

the layer has a thickness of approximately three to twelve nanometers; and

the substrate is a delta-doped, heteroepitaxial semiconductor substrate comprising:

a support layer comprised of semi-insulating gallium arsenide;

a buffer layer comprised of gallium arsenide overlying the support layer;

a doping layer delta-doped with silicon and overlying the buffer layer;

a spacer layer comprised of gallium arsenide and overlying the doping layer;

an channel layer comprised of indium gallium arsenide and overlying the spacer layer; and

a barrier layer comprised of aluminum gallium arsenide and overlying the channel layer, the barrier layer forming the surface for the delta-doped, heteroepitaxial semiconductor substrate.

25. The semiconductor component of claim 24 further comprising:

source and drain regions in the substrate;

a multi-layered spacer adjacent to the gate contact; and

source and drain contacts overlying the source and drain regions.